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IN THE UNITED STATES PATENT & TRADEMARK OFFICE

Attorney Docket No.: AUS920030655US1

Re Application of:

JUAN-ANTONIO CARBELLO

Serial No.: 10/687,257

Filed: OCTOBER 16, 2003

For: CHANNEL-BASED
TESTING OF
COMMUNICATION LINK

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Examiner: BURD, KEVIN MICHAEL

Confirmation No.: 9980

Group Art Unit: 2611

INFORMATION DISCLOSURE STATEMENT
PURSUANT TO 37 C.F.R. § 1.97

Commissioner for Patents
PO Box 1450
Alexandria, Virginia 22313-1450

Sir:

Applicants submit the following information on (Substitute) Form PTO-1449 listing references pursuant to 37 CFR 1.97. Hard copies of the patent references listed on (Substitute) Form PTO-1449 are included.

Please charge the fee of \$180.00 due under 37 CFR § 1.17(p) and any additional fees required for prosecution of the present application to **IBM Corporation Deposit Account no. 09-0447**.

Respectfully submitted,

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Substitute for form 1449/PTO

**INFORMATION DISCLOSURE
STATEMENT BY APPLICANT****Complete if Known**

Application Number	10/687,257
Filing Date	OCTOBER 16, 2003
First Named Inventor	JUAN-ANTONIO CARBELLO
Examiner Name	BURD, KEVIN MICHAEL
Art Unit	2611
Attorney Docket No.	AUS920030655US1

Examiner Initials	Document Number	Publication Date MM-DD-YYYY	Name of Patentee or Applicant of Cited Document	Pages, Columns, Lines, Where Relevant Passages or Relevant Figures Appear
	US 7,093,172	08/15/2006	FAN ET AL.	

FOREIGN PATENT DOCUMENTS

Examiner Initial	Foreign Patent Document	Publication Date MM-DD-YYYY	Name of Patentee or Applicant of Cited Document	Pages, Columns, Lines, Where Relevant Passages or Relevant Figures Appear

NON PATENT LITERATURE

Examiner Initial	Include name of author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc.), date, page(s), volume-issue number(s), publisher, city and/or country where published.
	Chen et al.; "A CMOS 400-MB/S SERIAL LINK FOR AS-MEMORY SYSTEMS USING A PWM SCHEME"; IEEE Journal of Solid-State Circuits; Vol. 36; No. 10; Oct. 2001; pages 1498-1505
	Yang et al.; "A 0.5- μ M CMOS 4.0 GBIT/S SERIAL LINK TRANSCEIVER WITH DATA RECOVERY USING OVERSAMPLING"; IEEE Journal of Solid-State Circuits; Vol. 33; No. 5; May 1998; pages 713-722
	Khoury et al.; "HIGH-SPEED SERIAL TRANSCEIVERS FOR DATA COMMUNICATION SYSTEMS"; IEEE Communications Magazine; Vol. 39; Issue 7; July 2001; pages 160-165
	Kim et al.; ADAPTIVE SUPPLY SERIAL LINKS WITH SUB-1V OPERATION AND PER-PIN CLOCK RECOVERY"; Computer Systems Laboratory, Stanford University; ISSCC 2002
	J.L. Eisenbies; "CONVENTIONS FOR DIGITAL DATA COMMUNICATION LINK DESIGN"; IBM Systems Journal; Vol. 6; No. 4; 1967; pages 267-302
	Rallapalli et al.; "EMULATION OF A SPACE BASED INTERNET COMMUNICATION LINK: DESIGN AND IMPLEMENTATION"; ITTC-FY2003-24350-04; Sept. 2002; The University of Kansas Center for Research, Inc.
	Goldsmith; "DESIGN AND PERFORMANCE OF HIGH-SPEED COMMUNICATION SYSTEMS OVER TIME-VARYING RADIO CHANNELS"; Copyright 2004; University of California at Berkeley

Examiner:

Date Considered:

EXAMINER: Initial if reference considered, whether or not citation is in conformance with MPEP 609; Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant.